REPLACEMENT CLAIMS

Sub C3

36. (Amended) A memory cell comprising:

an electropolished patterned metal layer provided over a semiconductor substrate;

B1

a transistor in electrical communication with said electropolished patterned metal layer, said transistor including a gate fabricated on said semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate; and

a capacitor including an electrode, said electrode being in electrical contact with said source/drain region.